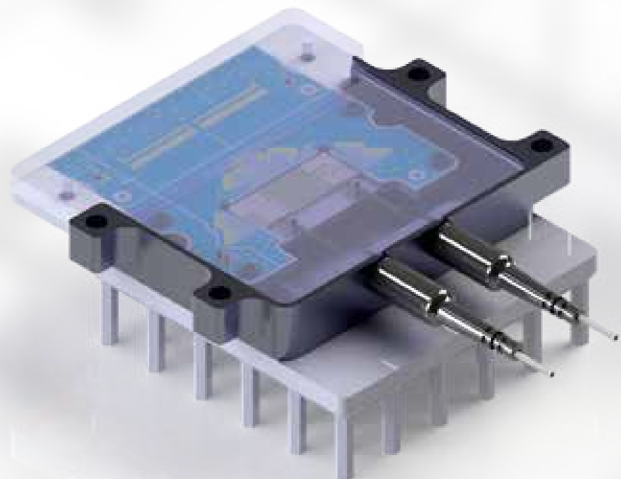
TEST, EVALUATE & PACKAGING OF PHOTONIC INTEGRATED CIRCUITS

- **Generic & Custom Packaging**
- **Support for InP, SOI an TriPleX PICs and modules**
- **Semi- & Fully-automated packaging equipment**
- **Dedicated and extremely experienced team**



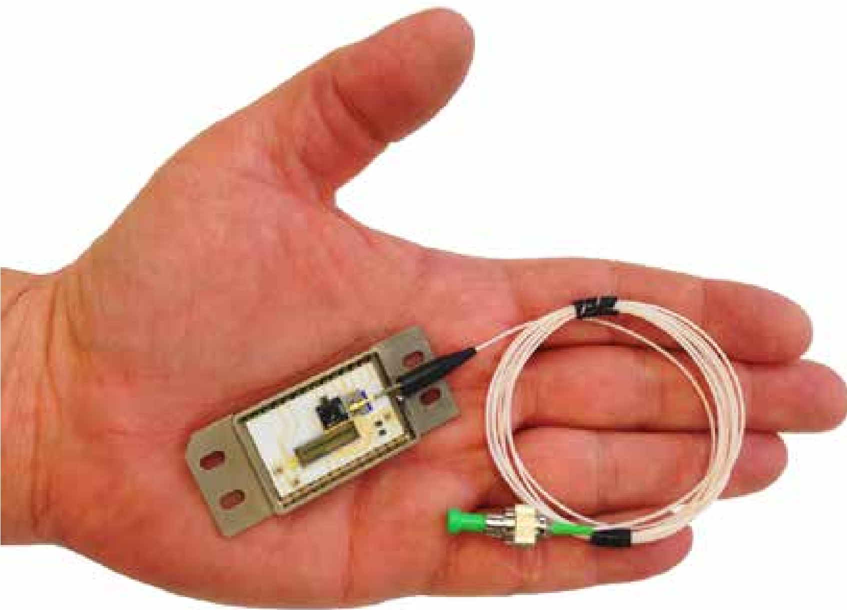
PIC TECHNOLOGY AS A GAME CHANGER

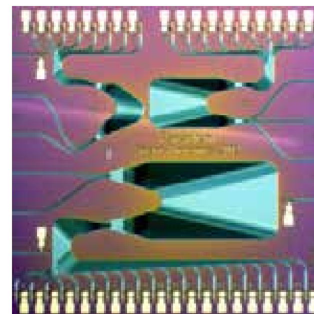
PIC technology is becoming more and more used for the next generation sensing and datacom equipment. The MPW-runs (Multi Project Wafer runs) offered by Jeppix TU/e, Fraunhofer HHI, LioniX, IMEC, LETI made it possible for SME companies to get affordable trials on InP, SOI and TriPleX wafer runs.

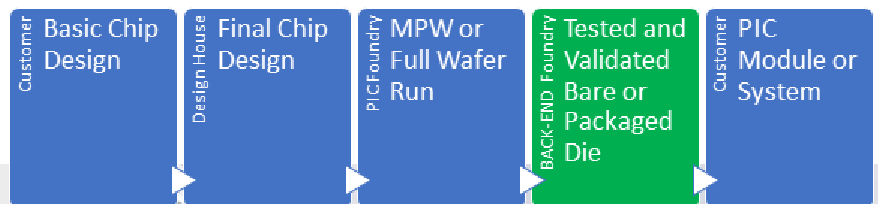
EXPERIENCE IN CHIP DESIGN TRAJECTORIES

Having standard building blocks available on the MPW runs may give the impression that designing a chip is straight forward, make your basic chip design, let a designer produce the real chip design, have a foundry produce the chips and you have your prototype ready. Reality is different. Your first chip will probably show some expected behaviours and it is seldom what you really want or what indicated by simulations. There are tweaks to be done on most designs.

With our extensive experience on chip design and long history with different foundries, we are in a excellent position to advise on the possible tweaks to be done on prototyping chips in order to minimize time and efforts during expansion in technological readiness level.

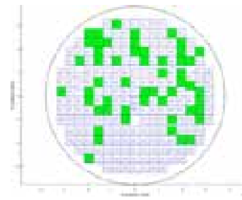


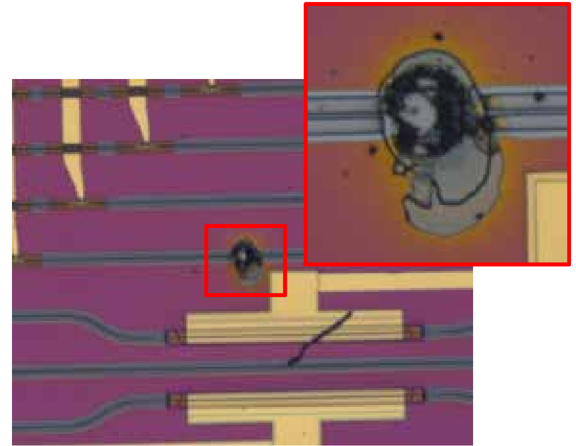




TESTING AND VALIDATION

Tipps invested steadily in testing and evaluation tools. The full test sequence can be run internally. Starting with visual inspection, functional testing of the bare die, evaluation of the functionality, comparison with simulation model, reporting to the designers and foundries. Root cause analysis of unexpected effects or behaviour.

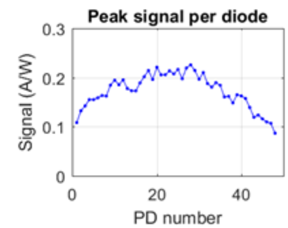


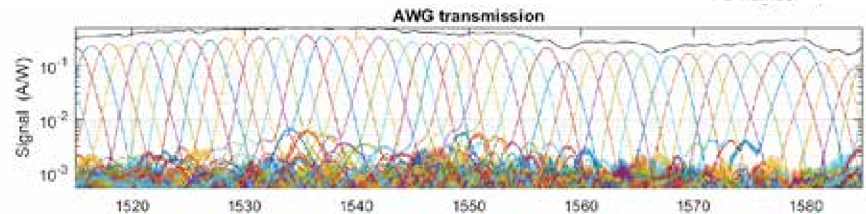


detected defect during visual inspection and yield evaluation

TEST AND VALIDATION OF BARE DIE

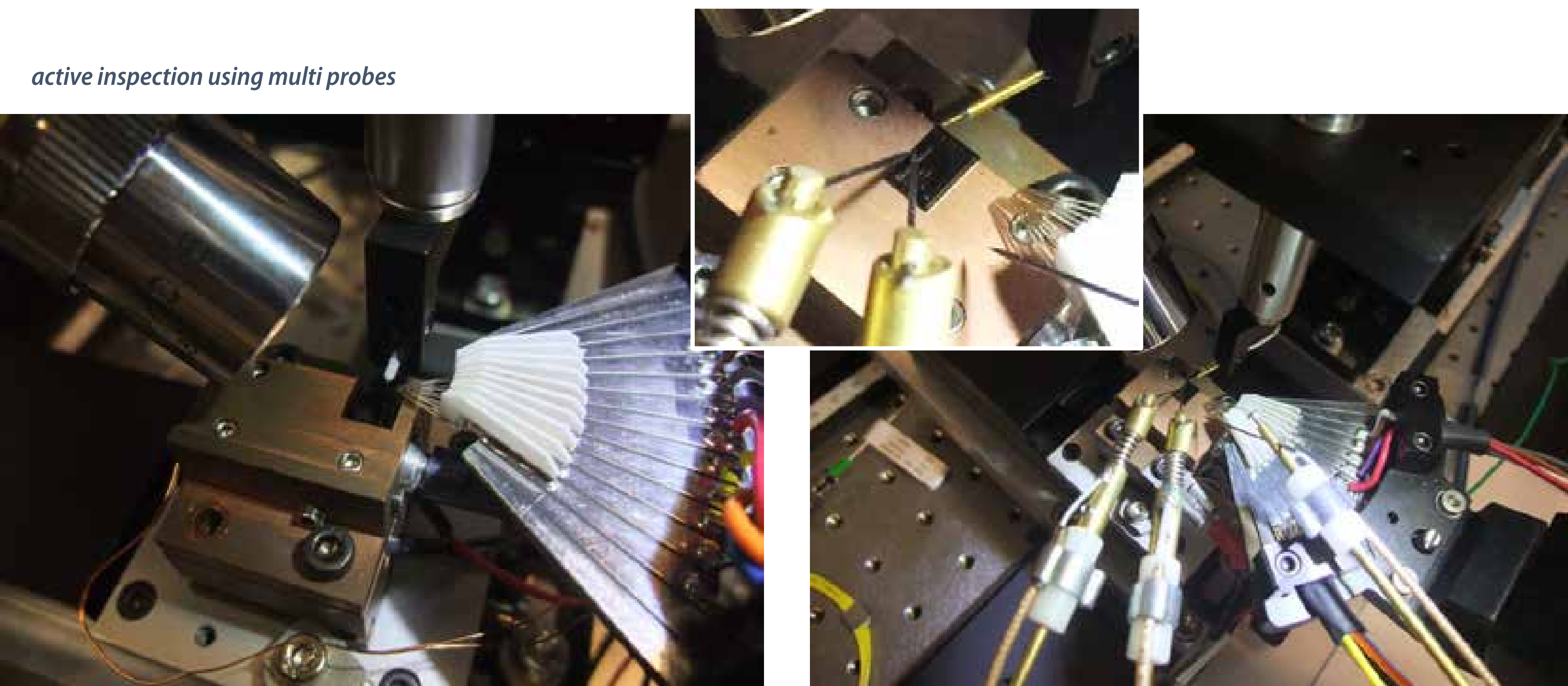
1. **Visual inspection**
   During the visual inspection of chip, defects like waveguide interruption, poor metallization, etc, can be identified.
2. **Functional testing**
   Our test benches are equipped with appropriate equipment and appliances for chip evaluation.
   With the multiprobe system, test chips with bondpads of pitch and dimensions in according with our 'General Design Rules for Packaging' can be tested for the transmission spectrum.
   Different type of optical I/Os (including SM or PM lensed or cleaved fibers and grating coupler) can be pigtailed to the test chips.
3. **Evaluation of the functionality**
   We have the right tools and software for data acquisition. Customers can evaluate the test results and the feedback from **Tipps** to determine whether the test chips are functioning as expected and provide the basis to decide on proceeding with packaging.
4. **Compare to the simulation model**
5. **Reporting to the designers and foundries**
6. **Root cause analysis of unexpected effects or behaviour**





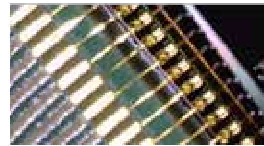
transmission test results

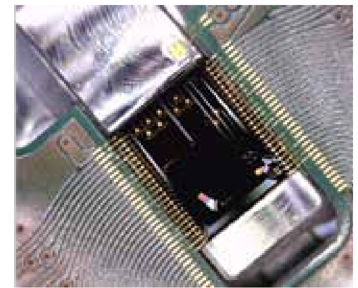
active inspection using multi probes



TEST AND VALIDATION OF PACKAGED DIE

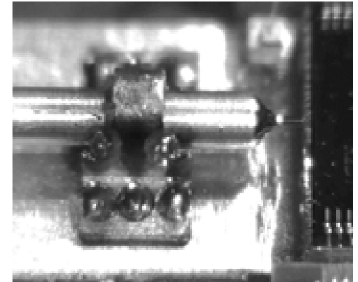
1. **Die bonding**
   Die-bonding refers to adhesion of chip to a fixed structure within the package and underneath the fixed structure there is the element for active cooling to control chip temperature up to sub-kelvin or even milli-Kevin scale. For precise positioning of chip and repeatable die-bonding quality, **Tipps** uses die-bonder to dispense the right amount of epoxy and pick-and-place chips.





consistent wire bond quality

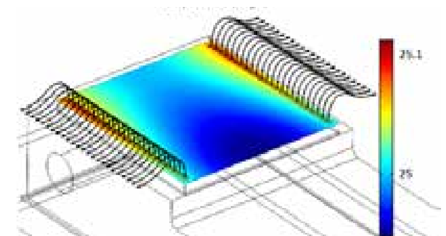
2. **Oven curing**
   Oven curing is being used for curing of epoxy and our programmable oven allows curing with different recipes to fit the different chip and package requirements. In some applications (e.g. Grating coupler) requires the use of UV curing epoxy and we have tunable UV sources for such applications.



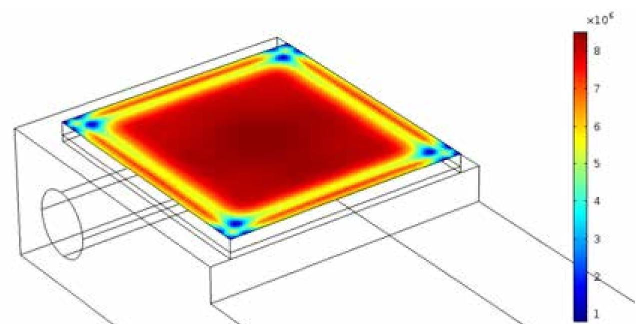
welding of fiber after active alignment to chip

3. **Wire bonding**
   Optical chips are connected to electronics world through gold wire connections. Wire-bonder is used to drawn these wires from metal bond pads on chip to bond pads on PCB.

4. **Fiber alignment**
   To minimize insertion loss from fiber to chip, we are equipped with semi-automatic fiber aligner which is capable of aligning fiber up to sub-micron precision, through active alignment.



temperature profile (above) and residual stress (below) on PIC



FOCUS ON HIGH PERFORMANCE

Packaging of PIC's is far more critical for the chips than packaging of electronic chips. Internal stresses, temperature fluctuations, temperature gradient on the chip, all contribute to changes in functionality of the chip after packaging. At **Tipps** we designed packages that will maintain the functionality of the chip after being packaged and will fit different requirements.

RAMP UP THE ECO SYSTEM

Tipps offers support to new players on the PIC technology field. In order to grow the eco system faster, we help companies to start working with PIC technology.

WE STRONGLY BELIEVE THAT TIPPS CAN HELP COMPANIES TO REDUCE THEIR NUMBER OF ITERATIONS SIGNIFICANTLY

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